

Alternative 64-bit CPUs inside Intel

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Abstract. *The Itanium Processor is a native 64 Bits processor based on IA-64 (Intel Architecture, 64 bit) that implements the EPIC (Explicit Parallel Instruction set Computing) architecture. Itanium uses a combination of techniques to improve the speed and performance, using the compiler to turns sequential code into parallelized 128-bit bundles that can be processed in the CPU without need to interpret it after. This allows the processor to concentrate on executing parallel code as fast as he can, without further optimizations or interpretations, having in this way more time to concentration on others tasks like parallelism executions.*

1 – Introduction

Intel leader of the market of processors since beginnings of the years ninety has put in office in the inquiry and development of new processors based in innovative architectures. In 1994, Intel began his work in a project called Merced (Itanium Code Name During development), project this that would represent Intel mark in the world of the processors 64-Bits. The processor Itanium, code-name Merced, was developed in a consortium between the Intel and HP, marking a break in the operation base with the processors up to that time developed, basically leaving for backwards the traditional forms of action of the CPUs on execution an operation of each time, as well as, surpasses level with architecture the needs of utilization of "tricks" of engineering for increase the processor speed, worry this that has occupied the engineers over the years. The philosophy adapted to delivery Itanium in the market was the same as other Motorola has made years ago in development of 16 to 32 bit processors. Unfortunately for Intel, the Itanium was a commercial failure because they tried a complete break with the past, not offering compatible mode to 32bit. With the AMD 64Bit Processors in the market giving both execution modes 32/64 Bit, Intel starts loosing market place for AMD. This obliged Intel it recoil in his strategy of market throwing in the market the processor with the technology EM64T¹, technology based in IA-32 but with improvements to work at 64bit mode. The first Intel Processor with this technology was Xeon Family Processors. With both EM64T and AMD64 based processors disputing the market, Intel still developing new processors technology and new approach's to processors architecture.

¹ EM64T – EXTENDED MEMORY 64 TECHNOLOGY

After some years without any news about Itanium, Intel presents to the market, again, the “new architecture” implemented in Itanium Family Processors they called EPIC²

2 – Itanium Features

Itanium Architecture have native 64Bit Computing and it uses an architecture called EPIC. The motivation for EPIC was the verification that the advancements of performance computational were deeds at the expense of a big increase in the complexity of the hardware. Others architecture approaches like VLIW permitted to solve that problem relegating for the compiler, the work of determine the parallelism of the instructions, but the one of the limitations of the VLIW is that he exposes the internal architecture of the processor [7]. Any changes in the number or execution units require that the compiler be re-writing and all the software recompiled. The assembly instructions of the Itanium were conceived to permit the future members of the family of processors Itanium performs the same software without having compatibility problem [2].

The basic concepts of the EPIC implementation is that the compiler should be able to indicate explicitly in the instruction sequence the parallelism inherent rather than obliging the processor to reconstruct the serial or sequential operations. To allow the compilers programmers to use the instruction-level parallelism (ILP) the architecture offers some helpful features [3]:

Predication — Instead of waiting for conditional branches (if/then) to be resolved, the processor can execute both branches simultaneously reducing this way branches needed. In the branch predication Itanium processor minimizes takes both possible paths to the next branch, where it follows both branches again. When it comes to the correct result it drops the other branch path that it doesn't need, keeps the branch that it does and it continues on with the calculation.

Speculation — Data can be loaded before the load command occurs in the instruction code, which can substantially reduce memory latencies, the data is dynamically checked when the actual load command occurs, and updated if necessary. This technique reduces the memory latency.

² EPIC Explicitly Parallel Instruction Computing is a 64-bit microprocessor instruction set, jointly defined and designed by Hewlett Packard and Intel, that provides up to 128 general and floating point unit registers and uses speculative loading, predication, and explicit parallelism to accomplish its computing tasks.

Software Pipelining — Software loops are a core element in many applications. The “traditional” architecture unrolls software loops to create multiple copies. With its many registers, EPIC can recognize and execute multiple loop iterations in parallel.

Out-of-Order Memory Optimization — Intel Itanium can explicitly enforce in-order memory access when needed. This enables significant performance optimizations.

In the ILP parallelism, Itanium separates de instructions bundles (128 bits each), with always three instructions per bundle for parallel execution and can execute two bundles per clock. Itanium Architecture provides mechanisms like instruction templates to permit the compiler to communicate with the processor in compilation time. Ref: [1 (302-307)]

Executions Units and Instructions Types: Ref: [1 (85-88)]

Itanium instructions are 41 bits wide and are always fetched in bundles of three, with 5 bit for template additional information. To increase speed taking advantage of parallelism, Itanium separates into Four(4) execution units types: M, F, I, B that executes six(6) different major instructions classes(A,I,M,B,F,X).

Operation	Instruction Type	Execution Units Type
Aritmetic, Logic Comparison	A	I, M, other avaiaable
Non-Alu Integer Operations	I	I
Memory Acess	M	M
Branches and Calls	B	B
Floating. Point Operations	F	F
Extended two-slot Instructions	X	I,B, depending of the Op.

Itanium Operations, Instructions and Execution Units Types

Registers and RSE: Ref: [1 (199-201), 3]

Itanium architecture has 128 registers which 32 registers are fixed and 96 are stacked in memory but used in fixed has they are needed [8]. A procedure call can allocate up to 96 of the stacked registers and still have access to the 32 common registers. Each procedure has its own register frame, which is flexible in size and because most of them procedure calls allocate only a few new registers, many calls can be made before the physical limits exceeded. A dedicated piece of hardware called the RSE (Register Stack Engine) will automatically clean older registers to free space in the register stack for the new requests. The RSE will also restore spilled registers as needed.

Registers Width:

128 Integer – 64Bit

128 General - 64Bit
128 Float-point – 82 Bits
8 Branch Registers – 64Bit
64 Predicate Registers - 1

Instruction Point register is a 64Bit Register than contains the bundle address.

Processor Pipeline:

To pipeline of the Itanium is constituted by 8 stages in-order, that perform in simultaneous 6 instructions (2 bundles). To perform the 6 instructions in parallel it uses 11 units of execution. These units find it self divided in 4 units of memory, 2 of entire, 2 of floating point and 3 of branch. The two first phases of the pipeline, front-end, healthy utilized for carry out the fetch of the instructions before of will be utilized by the back-end. There is a buffer of instructions that going to keep 8 bundles for utilization. Combining this buffer with the caches, this will decrease latency and a good system of branch prediction. [8]

3 – Technical Data

Itanium was initially released at 733MHz and 800MHz. It uses a three-stage caching system:

- 32K L1 (16K data and 16K code)
- 96K L2, 6-cycle latency
- Either a 2MB or 4MB L3 - 21- to 24-cycle latency.

With EM64T processors recently supporting high megahertz above 3000, the 800MHz (now Itanium 2 hits 1.6GHz) clock speed may seems to slow. However, the large I/O capabilities of Itanium allow it to perform millions of instructions at once using a fully optimised 64-bit applications and his EPIC architecture.

Contrary to the EM64T processors that are based in a IA-32 with stretches for the Intel 64 (the Intel EM64T 64bits), the Itanium incorporates the 64bit natively and gives support for the execution in way of “IA-32” through an emulation incorporated in the processor. This gave Intel the option to prepare them commercial future in the world of Native 64-Bits processors. Itanium 2 has some new capabilities and improvements compared to his first version. Has we can see in the next table.

Table 1. Features of the Itanium 2 processor.		
Design		
Frequency	1 GHz	
Pipe stages	8 in-order	
Issue/retire	6 instructions	
Execution units	2 integer, 4 memory, 3 branch, 2 floating-point	
Silicon		
Technology	180 nm	
Core	40 million transistors	
L3 cache	180 million transistors	
Size	421 mm ²	
Caches		
L1 instruction	Size	16 Kbytes
	Latency	1 cycle
	Protection	Parity
L1 data	Size	16 Kbytes
	Latency	1 cycle
	Protection	Parity
L2	Size	256 Kbytes
	Latency	5, 7, or 9+ cycles
	Protection	Parity or ECC*
L3	Size	3 Mbytes
	Latency	12+ cycles
	Protection	ECC

[6]Image from www.uiuc.edu

4 – Conclusion

Itanium systems operate directly on 64-bit integer and floating point data. 64-bit integers, for instance, provide the ability to operate large numbers on one operation, improving performance for operations such as databases and data mining centres. Since many tasks can be completed in a single 64-bit operation instead of two 32-bit operations, Itanium based systems provide greater performance at the same clock rate of the EM64T processors. EPIC try to be a computer mix techniques to use at maximum the parallelism execution. With the competition from AMD, Intel is trying to put in the market one processor that can take advantage not only of the hardware but a mix techniques used in Hardware and Software. Intel is preparing Itanium has to be the processor computer support for high-end companies, while will support EM64T processors for the other segment of the market.

References

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