Mestrado em Informática

2009/10

A.J.Proença

Tema

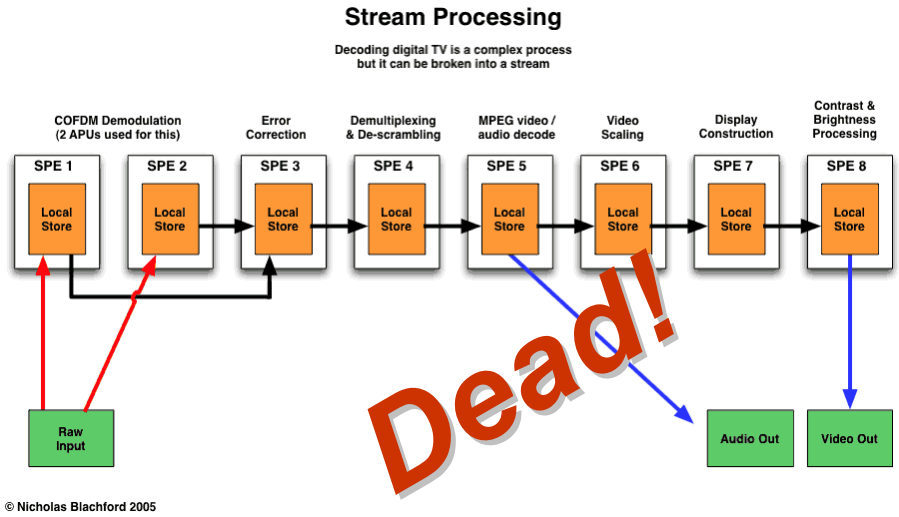
Arquitecturas Paralelas (3)

Adaptado de

Intel website and other websites

- Composed of a non-SMP architecture
  - 234M transistors @ 4Ghz
  - 1 Power Processing Element (PPE) "control" processor. The PPE is similar to a Xenon core
    - Slight ISA differences, and fine-grained MT instead of real SMT
- And 8 "Synergistic" (SIMD) Processing Elements (SPEs)
  - An attempt to 'fix' the memory latency problem by giving each SPE complete control over it's own 256KB "scratchpad" memory
    - Direct mapped for low latency
    - 4 vector units per SPE, 1 of everything else – 7M transistors
  - 512KB L2$ and a massively high bandwidth (200GB/s) processor-memory bus

Dead!



Estrutura do tema AP

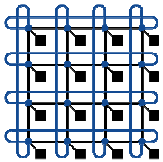
1. A evolução das arquitecturas pelo paralelismo
2. Multiprocessadores (SMP e MPP)
3. Data Parallelism: SIMD, Vector, GPU, …
4. Topologias de interligação

Multiprocessor Network Topologies: Interconnection Networks

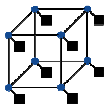
- Network topologies
  - Arrangements of processors, switches, and links

Bus

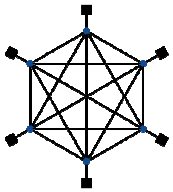
Ring



2D Mesh

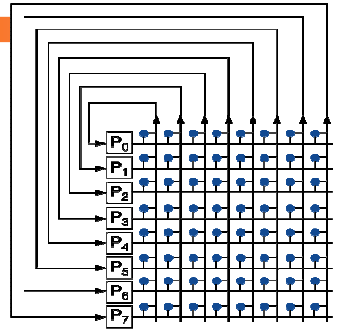


N-cube (N = 3)

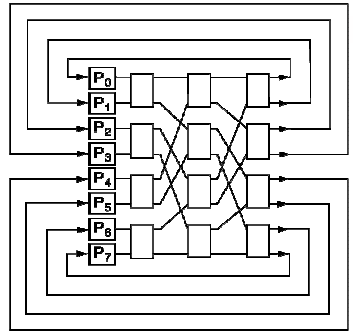


Fully connected

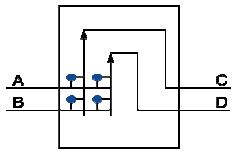
Multistage Networks



a. Crossbar



b. Omega network



c. Omega network switch box

Network Characteristics

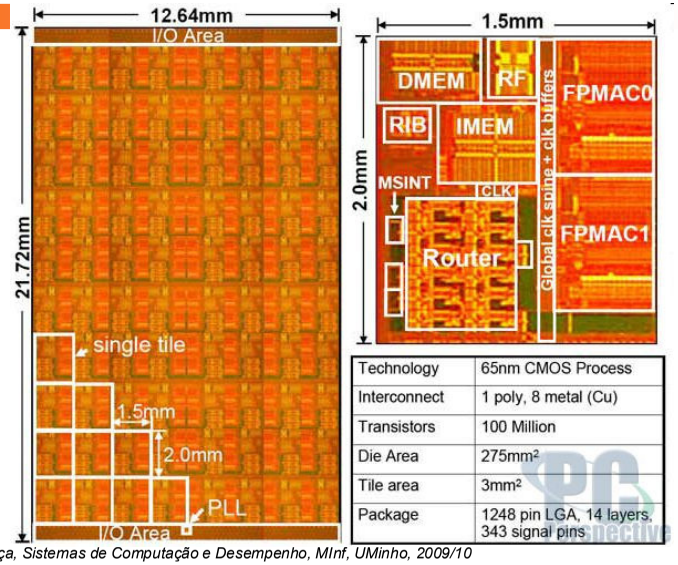
- Performance
  - Latency per message (unloaded network)
  - Throughput
    - Link bandwidth
    - Total network bandwidth
    - Bisection bandwidth
  - Congestion delays (depending on traffic)
- Cost
- Power
- Routability in silicon

Arquitecturas Paralelas

Estrutura do tema AP

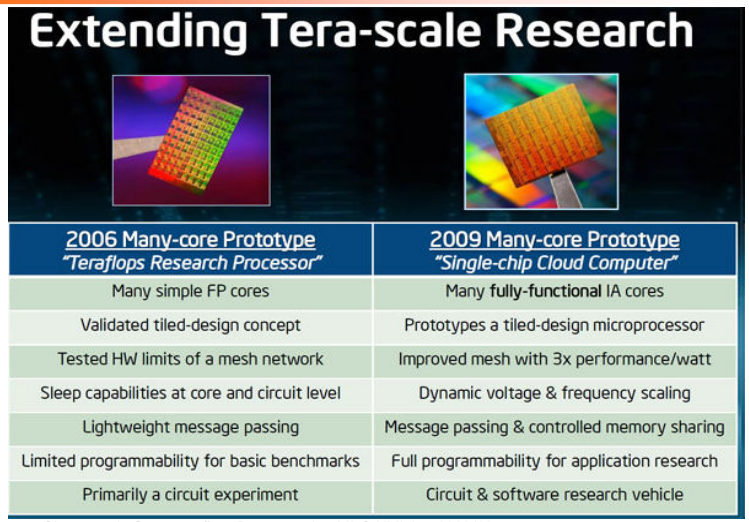
1. A evolução das arquitecturas pelo paralelismo
2. Multiprocessadores (SMP e MPP)
3. Data Parallelism: SIMD, Vector, GPU, …
4. Topologias de interligação
5. Evolução dos many-cores na Intel

Back in 2007, the 80-core promise



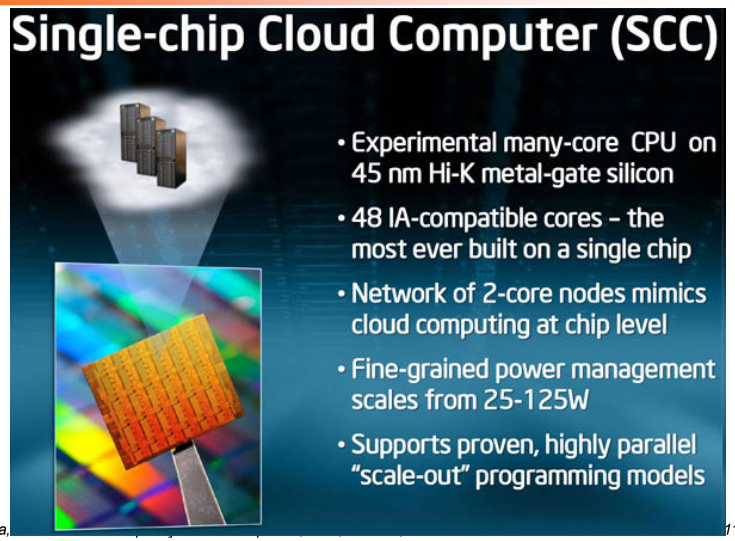
Technology	65nm CMOS Process
Interconnect	1 poly, 8 metal (Cu)
Transistors	100 Million
Die Area	275mm²
Tile area	3mm²
Package	1248 pin LGA, 14 layers, 343 signal pins

From 2006 to 2009

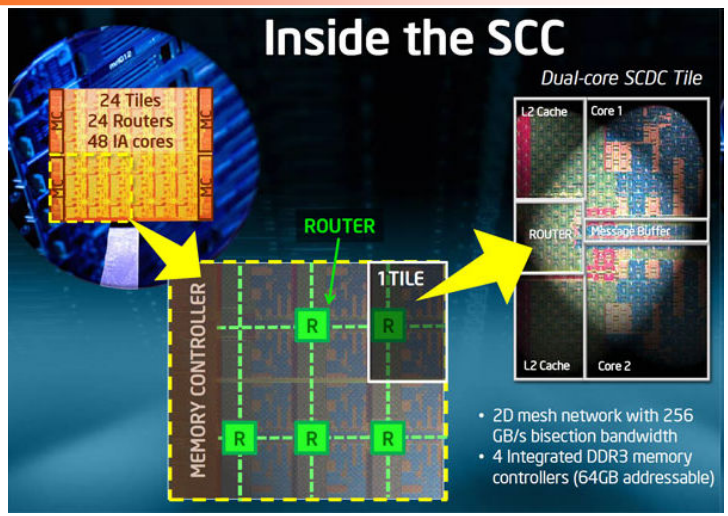


2006 Many-core Prototype "Teraflops Research Processor"	2009 Many-core Prototype "Single-chip Cloud Computer"
Many simple FP cores	Many **fully-functional** IA cores
Validated tiled-design concept	Prototypes a tiled-design microprocessor
Tested HW limits of a mesh network	Improved mesh with 3x performance/watt
Sleep capabilities at core and circuit level	Dynamic voltage & frequency scaling
Lightweight message passing	Message passing & controlled memory sharing
Limited programmability for basic benchmarks	Full programmability for application research
Primarily a circuit experiment	Circuit & software research vehicle

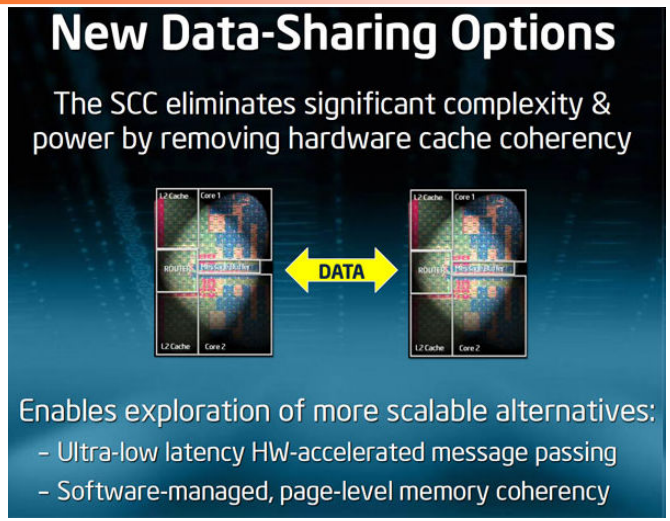
The SCC prototype



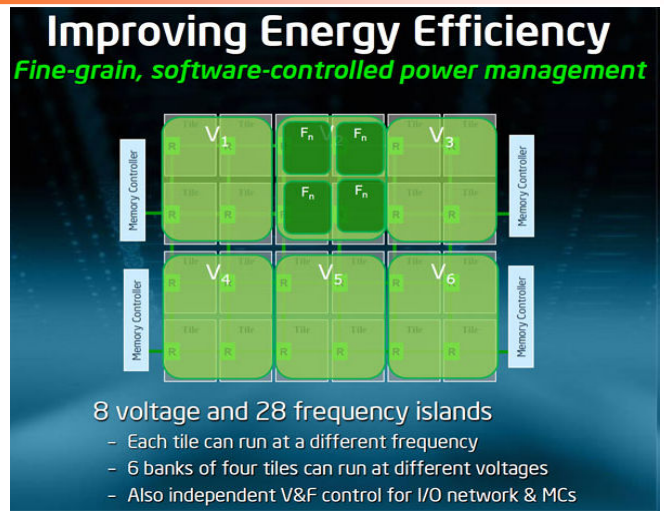
Internal architecture



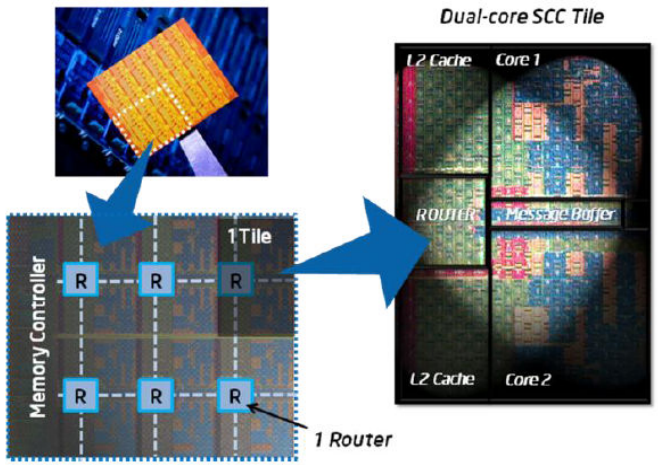
Move
from shared memory to message passing



Efficient energy management



Rewind



Source of information