

Mestrado em Informática

2009/10

A.J.Proença

Tema

Arquitecturas Paralelas (3)

Adaptado de

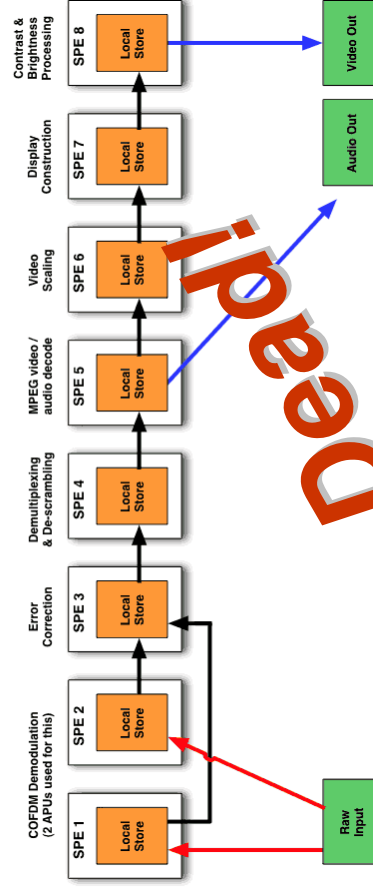
Intel website and other websites

- Composed of a non-SMP architecture
 - 234M transistors @ 4Ghz
 - 1 Power Processing Element (PPE), "control" processor. The PPE is similar to a Xenon core
 - Slight ISA differences, and fine-grained MT instead of real SMT
- And 8 "Synergistic" (SIMD) Processing Elements (SPEs)
 - An attempt to 'fix' the memory latency problem by giving each SPE complete control over it's own 256KB "scratchpad" memory
 - Direct mapped for low latency
 - 4 vector units per SPE, 1 of everything else – 7M transistors
 - 512KB L2\$ and a massively high bandwidth (200GB/s) processor-memory bus

How to make use of the SPEs

Stream Processing

Decoding digital TV is a complex process but it can be broken into a stream



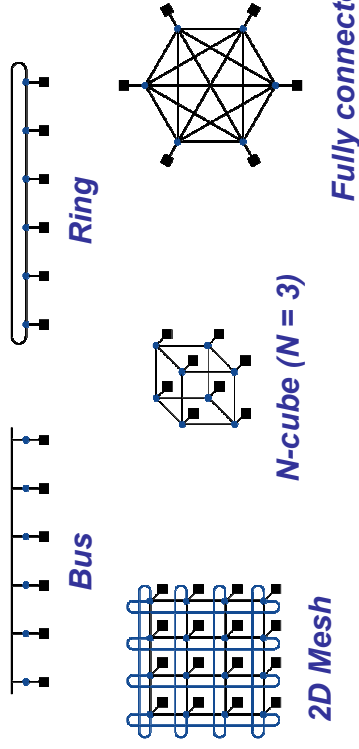
Arquitecturas Paralelas

Estrutura do tema AP

- A evolução das arquitecturas pelo paralelismo
- Multiprocessadores (SMP e MPP)
- Data Parallelism: SIMD, Vector, GPU, ...
- Topologias de interligação

Multiprocessor Network Topologies: Interconnection Networks

- Network topologies
 - Arrangements of processors, switches, and links



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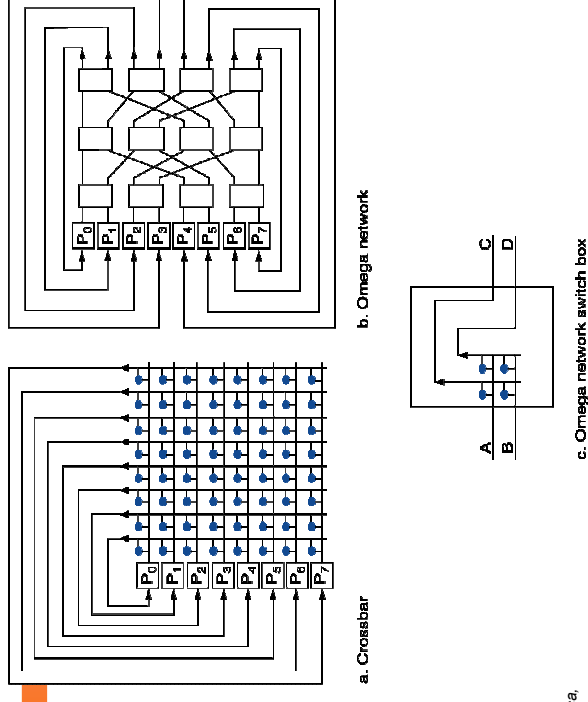
Network Characteristics

- Performance
 - Latency per message (unloaded network)
 - Throughput
 - Link bandwidth
 - Total network bandwidth
 - Bisection bandwidth
 - Congestion delays (depending on traffic)
- Cost
- Power
- Routability in silicon

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Multistage Networks



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Arquitecturas Paralelas

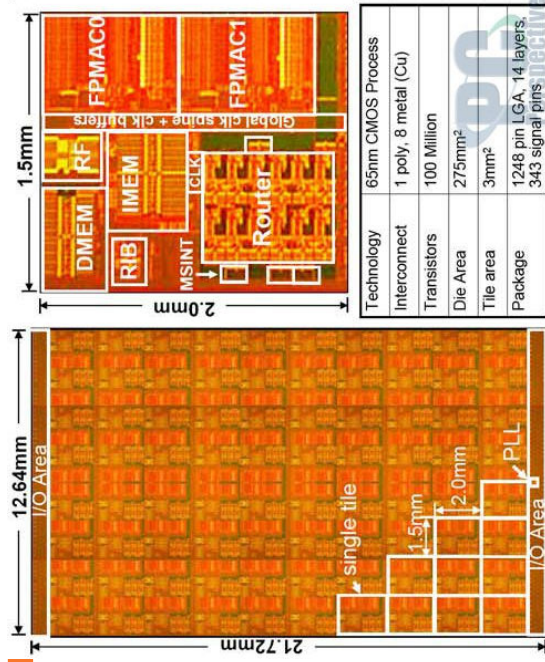
Estrutura do tema AP

1. A evolução das arquiteturas pelo paralelismo
2. Multiprocessadores (SMP e MPP)
3. Data Parallelism: SIMD, Vector, GPU, ...
4. Topologias de interligação
5. Evolução dos many-cores na Intel

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Back in 2007, the 80-core promise



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From 2006 to 2009

Extending Tera-scale Research



2006 Many-core Prototype "Teraflops Research Processor"	2009 Many-core Prototype "Single-chip Cloud Computer"
Many simple FP cores	Many fully-functional IA cores
Validated tiled-design concept	Prototypes a tiled-design microprocessor
Tested HW limits of a mesh network	Improved mesh with 3x performance/watt
Sleep capabilities at core and circuit level	Dynamic voltage & frequency scaling
Lightweight message passing	Message passing & controlled memory sharing
Limited programmability for basic benchmarks	Full programmability for application research
Primarily a circuit experiment	Circuit & software research vehicle

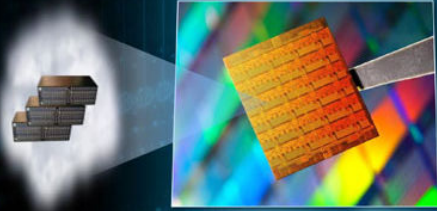
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The SCC prototype

Single-chip Cloud Computer (SCC)

- Experimental many-core CPU on 45 nm Hi-K metal-gate silicon
- 48 IA-compatible cores - the most ever built on a single chip
- Network of 2-core nodes mimics cloud computing at chip level
- Fine-grained power management scales from 25-125W
- Supports proven, highly parallel "scale-out" programming models

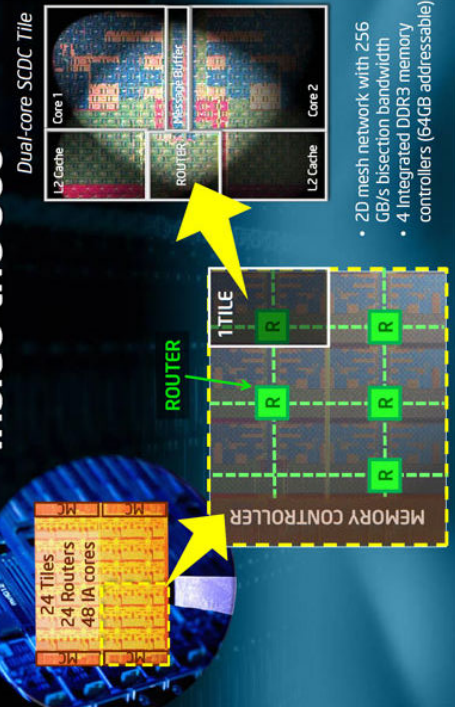


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Internal architecture

Inside the SCC



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Move
from shared memory to message passing

New Data-Sharing Options

The SCC eliminates significant complexity & power by removing hardware cache coherency



Enables exploration of more scalable alternatives:

- Ultra-low latency Hw-accelerated message passing
- Software-managed, page-level memory coherency

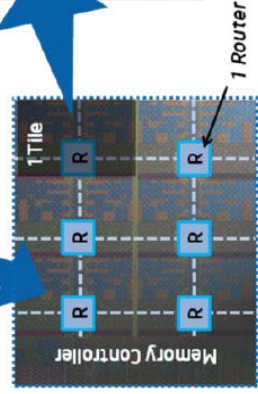
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Rewind



Dual-core SCC Tile



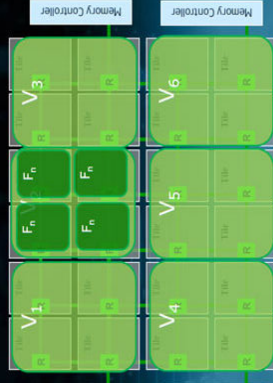
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Efficient energy management

Improving Energy Efficiency

Fine-grain, software-controlled power management



8 voltage and 28 frequency islands

- Each tile can run at a different frequency
- 6 banks of four tiles can run at different voltages
- Also independent V&F control for I/O network & MCs

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