W(i) = Write to line by processor i
R(i) = Read line by processor i
Z(i) = Displace line by cache i
W(j) = Write to line by processor j ($j \neq i$)
R(j) = Read line by processor j ($j \neq i$)
Z(j) = Displace line by cache j ($j \neq i$)

Note: State diagrams are for a given line in cache i

Figure 16.20 Two Cache Coherence Protocols