8	16	16	16
Add	B	C	A

Memory-to-Memory
I = 56, D = 96, M = 152

8	4	16		
Load	rB	B		
Load	rC	B		
Add	rA	rB	rC	
Store	rA	A		

Register-to-Memory
I = 104, D = 96, M = 200

(a) A ← B + C

8	16	16	16
Add	B	C	A
Add	A	C	B
Sub	B	D	D

Memory-to-Memory
I = 168, D = 288, M = 456

8	4	4	4
Add	rA	rB	rC
Add	rB	rA	rC
Sub	rD	rD	rB

Register-to-Memory
I = 104, D = 96, M = 200

(b) A ← B + C; B ← A + C; D ← D – B

I = Size of executed instructions
D = Size of executed data
M = I + D = Total memory traffic

Figure 12.5 Two Comparisons of Register-to-Register and Memory-to-Memory Approaches