UltraSparc-III

vs

Intel IA-64

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UltraSparc-III vs Intel IA-64

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Introduction

- UltraSparc-III (US-III) is the third generation from the UltraSPARC family of Sun
- Is a RISC processor and uses the 64-bit SPARC-V9 architecture
- IA-64 is Intel's extension into a 64-bit architecture
- IA-64 processor is based on a concept known as EPIC (Explicitly Parallel Instruction Computing)

Framework Definition

- **Reliability**
- **Instruction level Parallelism (ILP)**
  - instructions per cycle
- **Branch Handling**
  - Techniques:
    - branch delay slots
    - predication
  - Strategies:
    - static
    - dynamic

Framework Definition

- **Memory Hierarchy**
  - **main memory and cache memory**
  - **cache levels location**
  - **cache organization:**
    - fully associative - every entry has a slot in the "cache directory" to indicate where it came from in memory
    - one-way set associative - only a single directory entry be searched
    - two-way set associative - two entries per slot to be searched (and is extended to four-way set associative cache)
  - **memory latency**

Framework Definition

- **Pipeline**
  - increase the speed of CPU processing
  - several stages that performs part of the work necessary to execute an instruction
- **Instruction Set (IS)**
  - is the hardware "language" in which the software tells the processor what to do
  - can be divided into four basic types of operations such as arithmetic, logical, program-control and load and store operations, with a certain format.

Architecture Comparition - Reliability

- US-III performs advanced error detection and correction system
  - L2 cache offers full ECC (error checking and correction) capabilities
  - data parity bit protection with the ability to detect and correct single bit errors
  - automatic recovery system minimizes the impact of errors
- IA-64 has Machine Check Architecture (MCA) and Error Correcting Code (ECC) to help provide advanced error detection, containment, and correction as well as error logging

Architecture Comparition - ILP

- US-III
  - maintains a sustainable issue rate of 4 instructions every clock cycle
  - 16 fetched instructions can be queued up, waiting for an appropriate execution unit to become available
  - has six parallel execution units: 2 integer ALUs (both identical), 1 branch unit, 1 load/store unit, and 2 floating-point units (1 for add/subtract, 1 for multiply/divide operations)
  - contains independent execution units for different operations
- IA-64
  - use a 128-bit encoding: bundle (41-bit instructions and 5-bit template field)
  - issue a maximum of six instructions per clock cycle

Architecture Comparition - Branch Handling

- US-III
  - fully static branch prediction.
  - branch delay slots technique
  - 4-entry branch miss queue
- IA-64
  - dynamic branch prediction
  - predication technique
  - software hints to improve hardware use prediction and prefetching resources
  - explicit support for software pipelining of loops and exist prediction of counted loops

Architecture Comparition - Memory Hierarchy

- US-III
  - two cache units (L1 and L2)
  - L1: four separate caches
  - L2: single large cache
  - cache location
  - cache size
  - 4-way set associative architecture
  - integrates the system memory controller directly into the CPU's core
  - 3.2GB/s of CPU-to-memory bandwidth

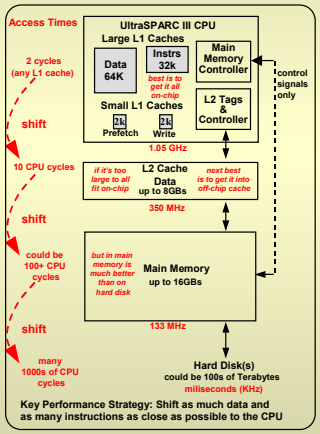

Fig. 1 - UltraSparc-III Memory Hierarchy

Architecture Comparition - Memory Hierarchy

- IA-64
  - three cache levels and a large registry set
  - L1 cache is 16 KB, 4-way set–associative and has 2-cycle latency
  - L2 cache is 96 KB, 6-way set-associative and has 6 or 9-cycle latency for INT or FP
  - L3 cache is 4 MB, off-chip, on-package, 4-ways, and has 21 or 24-cycle (INT or FP) latencies
  - large registry files: among others, 128 for integers, 128 for floating point, 8 branch registers, 64 1-bit predicate registers for use with predication

Architecture Comparition - Pipeline

- US-III processor execution pipeline is segmented into 14 separate stages
  - A through J - instruction issue unit
  - R through D - integer execution unit
  - E, C, M, and W - data cache unit in parallel with integer execution unit
  - E through D - floating-point unit
  - system interface unit and external memory unit have internal pipelines
- IA-64 processor: 10-stage in-order pipeline with cycle time designed for single cycle ALU (4 ALUs globally bypassed) and low latency from data cache.

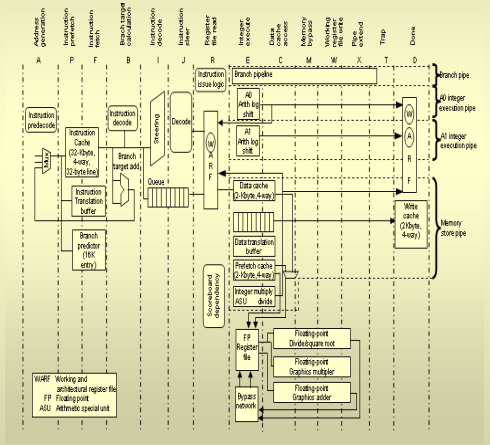

Fig. 2 - UltraSparc-III instruction pipeline

Architecture Comparition - IS

- US-III
  - integer data types that are signed and unsigned bytes (16, 32 and 64-bit)
  - floating-point numbers (32, 64 or 128 bits)
  - Visual Instruction Set (VIS)
  - divide standard floating-point graphic operations across the entire scope of the integer and floating-point execution units
  - special commands to complete normal CPU intensive graphic operations
- IA-64
  - four instructions categories: integer, load/store, floating-point, and branch operations
  - instructions fixed length: 128 bit (bundles)

Future Trends

- MAJC or "Microprocessor Architecture for Java Computing"
- the successor to the US-III , the UltraSparc IV will be offered at speeds beginning at 1.2GHz. The chip will include the capacity for instruction-level parallelism and thread-level parallelism
- Sun's product line also revealed that the UltraSparc V will first be offered at 1.8GHz speeds with the capacity to expand to 3.0GHz or higher
- the second IA-64 processor after Itanium is McKinley and it is likely to be faster, smaller, and all-around better than its predecessor
- next comes Madison, expected to be a 0.13-micron shrink of McKinley, all other things being equal
- Deerfield, the fourth member of IA-64's family, will also be a 0.13-micron shrink of McKinley, but with a smaller 1M L3 cache and yet another new bus interface intended for cheaper systems

Conclusions

- both processors aim mainly for server and workstation applications, focusing on improved capabilities and speed
- the US-III processor holds advantages in handling branches and integer operations also go in favor of US-III because of its faster clock speed, low instruction latency, and adequate number of execution units
- in terms of L1, US-III uses 64KB of data caching combined with 32KB of instruction caching while IA-64 has on the Level 1 a cache size of only 16KB
- in terms of L2, US-III incorporates 8Mb of L2 cache while the IA-64 is only 96KB in size
- IA-64 implementation of EPIC technology enables the compiler and hardware to work together efficiently to expose new levels of parallelism and performance
- both processors use speculative loading to help overcome memory latency problems but the way the two chips deal with exception errors differs slightly

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